**IN THE CLAIMS:**

Please amend the claims as follows.

**Claims 1-4 (canceled)**

5. (currently amended) A method of erasing a non-volatile memory cell with a nitride tunneling layer, ~~the non-volatile memory~~ comprising:

providing a non-volatile memory comprising a substrate, a nitride tunneling layer disposed on the substrate, a charge trapping layer having hot electron holes disposed on the nitride tunneling layer; and

~~a substrate;~~

~~a nitride tunneling layer disposed on the substrate;~~

~~a charge trapping layer having hot electron holes, disposed on the nitride tunneling layer;~~

~~a dielectric layer disposed on the charge trapping layer;~~

~~a gate conductive layer disposed on the dielectric layer; and~~

~~a source region and a drain region disposed in the substrate beside the gate conductive layer;~~

~~the method comprising the steps of:~~

applying a first positive bias to the drain region, applying a second positive bias to the gate conductive layer, and grounding the source region and the substrate, wherein hot electrons are injected into the charge-trapping layer through the nitride tunneling layer, and wherein said

hot electrons combine with electron holes in the charge-trapping layer to erase the non-volatile memory cell.

6. (original) The method of claim 5, wherein the first positive bias ranges from about 2V to about 5V.

7. (original) The method of claim 5, wherein the second positive bias ranges from about 2.5V to about 5V.

8. (previously presented) The method of claim 5, wherein the first positive bias and the second positive bias are both sufficient to erase the non-volatile memory.

9. (new) A method of erasing a non-volatile memory cell with a nitride tunneling layer, comprising:

providing a non-volatile memory comprising a substrate, a nitride tunneling layer disposed on the substrate, a charge trapping layer having hot electron holes directly in contact with the nitride tunneling layer; and

applying a first positive bias to the drain region, applying a second positive bias to the gate conductive layer, and grounding the source region and the substrate, wherein hot electrons are injected into the charge-trapping layer through the nitride tunneling layer, and wherein said hot electrons combine with electron holes in the charge-trapping layer to erase the non-volatile memory cell.

10. (new) The method of claim 9, wherein the first positive bias ranges from about 2V to about 5V.

11. (new) The method of claim 9, wherein the second positive bias ranges from about 2.5V to about 5V.

12. (new) The method of claim 9, wherein the first positive bias and the second positive bias are both sufficient to erase the non-volatile memory.